USRP-2955 Features

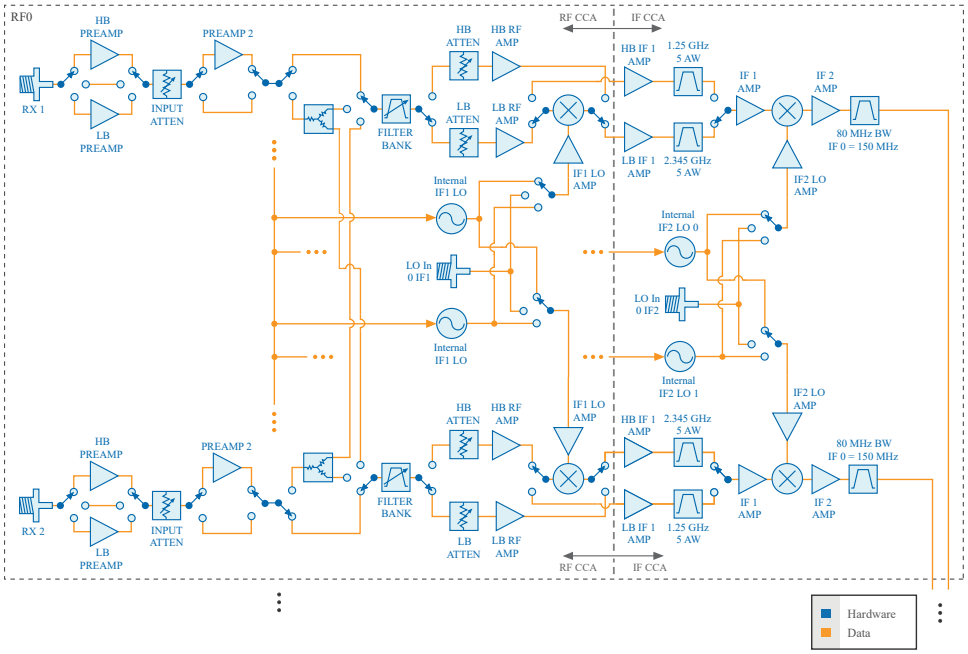
2026-11-11

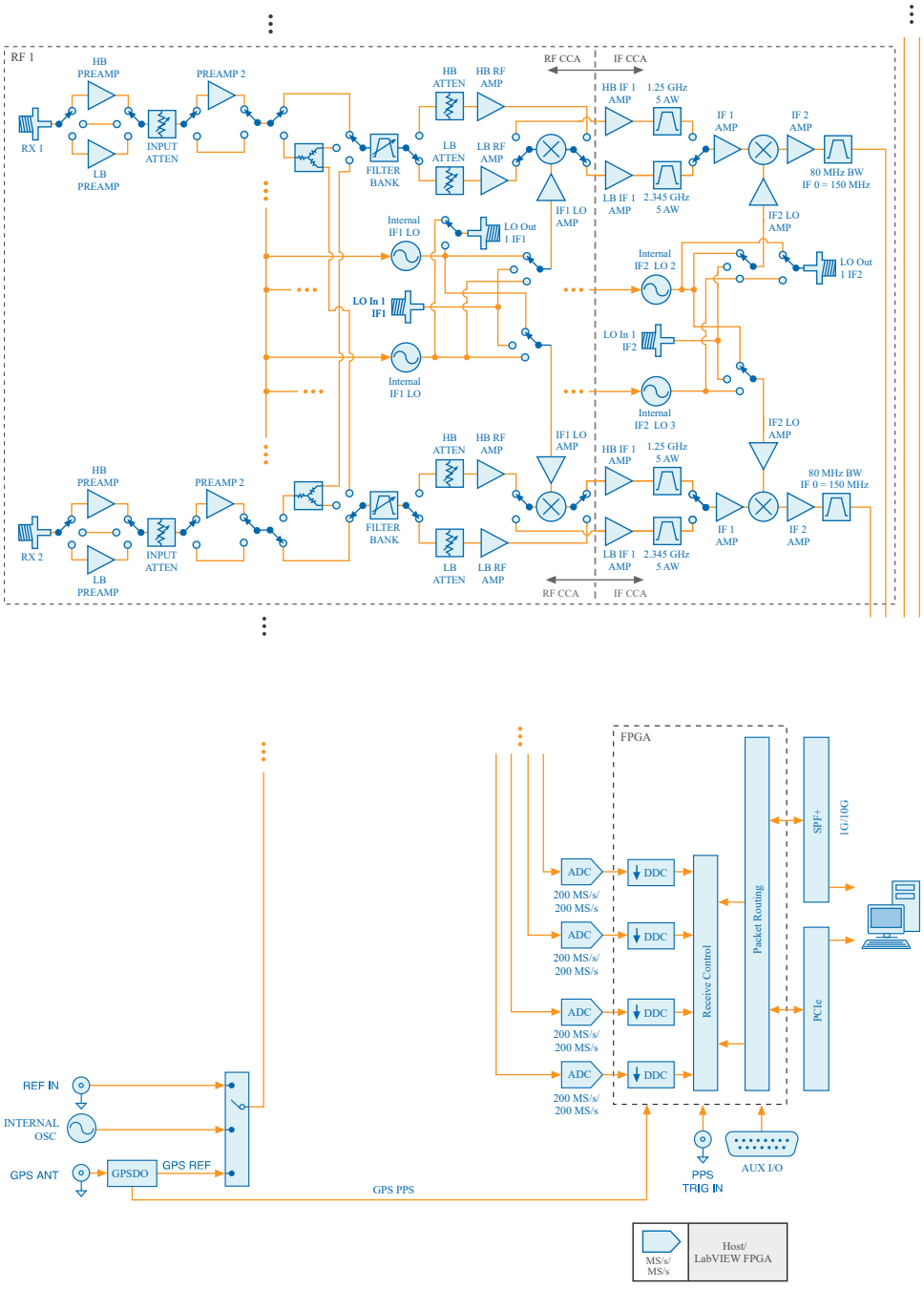
Contents

USRP-2955 Block Diagram 3

USRP-2955 Block Diagram

Signals received by the USRP-2955 are amplified, downconverted, filtered, digitized, and decimated before being passed to the host computer.





The following list describes the path of the individual blocks:

- Depending on the frequency of interest, the input signal is first amplified by a high-band (HB) or low-band (LB) pre-amplifier.
- The input attenuator attenuates the signal.
- Another pre-amplifier (pre-amplifier 2) amplifies the signal further.
- The filter bank filters the signal depending on the incoming frequency of interest.

- The HB or LB attenuator attenuates and amplifies the signal.
- The phase-locked loop (PLL) controls the voltage-controlled oscillator (VCO) so that the device clocks and local oscillators (LO) can be frequency-locked to a reference signal.
- The first mixer downconverts the signals to the Intermediate Frequency (IF) 1 frequency using either the internal IF1 LOs of either RX1 or RX2, or the LO IN 0 IF1 connector.
- Either the HB IF1 amplifier and the 1.25 GHz SAW filter, or the LB IF1 amplifier and the 2.345 GHz SAW filter amplifies and filters the IF 1 signal.
- The IF1 amplifier amplifies the signal.
- The signal is mixed with either the internal IF2 LOs of either RX1 or RX2, or the LO IN 0 IF2 connector.
- The IF2 amplifier amplifies the signal.
- The IF2 amplifier band-pass filters the signal for 80 MHz of bandwidth at IF2 (150 MHz) .
- The analog-to-digital converter (ADC) digitizes the IF2 signal.
- The digital downconverter (DDC) frequency-shifts, filters, and decimates the signal to in-phase/quadrature data (I/Q) at a rate you specify.
- The downconverted samples are transported to the host computer over a standard PCIe connection.

© 2026 National Instruments Corporation.